Logic Folding and Fine-Grained Logic-on-Logic 3D ICs: A Key Enabler of Tau Law

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Abstract:

Fine-grained 3D ICs distribute individual logic gates across multiple tiers using a logic-on-logic stacking architecture, enabling a level of integration beyond conventional memory-on-logic designs. This approach has demonstrated superior power, performance, and area (PPA) compared with coarse-grained 3D integration, and recent processors employing Logic Folding exemplify its growing adoption. Fine-pitch bonding technologies, such as face-to-face hybrid bonding, have made fine-grained 3D ICs practical. Realizing their full potential, however, requires advanced physical design methodologies that co-optimize millions of gates across tiers while efficiently managing millions of hybrid-bond interconnects. In this talk, we present novel algorithms and methodologies for physical design and multi-physics analysis of fine-grained 3D ICs, achieving significant PPA improvements over both coarse-grained 3D ICs and state-of-the-art 2D designs. We also discuss AI EDA techniques for reducing cross-tier connectivity while preserving PPA and improving yield, manufacturability, and testability.